International Journal of Recent Innovations in Academic Research
E-ISSN: 2635-3040; P-ISSN: 2659-1561
Homepage: https://www.ijriar.com/
Volume-9, Issue-3, July-September-2025: 149-152

Research Article

Innovative "Multi-Layered Glass Chip" (Glass Plus Polysilicon Chip) as the New Standard for the Future of the Computer Industry

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Received: July 08, 2025 **Accepted:** July 28, 2025 **Published:** August 04, 2025

Abstract
According to Moore's Law in the computer science community, the size and processing power of chips will halve every 18 to 24 months, while computing power will also double. Experts generally predict that nanochips will appear in the near future, and their size will be 100 to 1,000 times smaller than it is now. However, in recent years, the development time for each generation of chips has been getting longer and longer, that is, the development speed has slowed down. The time it takes for chip generations to change is longer than Moore's Law, indicating that Moore's Law has been surpassed. It also means that traditional methods of researching, designing, and manufacturing chips have become outdated, requiring new standards and new raw materials for processing. Therefore, this article hopes to propose a new innovative concept in chip construction methods that combines the concept of chip multi-layering, and use new semiconductor materials to create a new type of "glass core" multi-layer chip. We hope to make a contribution to the industry and even the computer community.
Keywords: Multi-Layered Glass Chip, Glass Plus Polysilicon Chip, Chip Multi-Layering Compression, Moore's Law.

Introduction

The history of computers dates back to the 1940s. The first computer was invented in 1947 at Bell Laboratories in the United States. It used transistors to perform operations on zeros and ones. This computer could be considered a large electronic computer. In the 1960s, three engineers struck out on their own and founded Fairchild Semiconductor. The transistor, the first integrated circuit, was invented. Chip miniaturization set the trend at this time, and Moore's Law has since become the foundation of the industry. Data analysis shows that the growth rate of the number of transistors in computer processors over the past 60 years has been consistent with the predictions of Moore's Law, indicating that the baseline design direction and solutions established by the industry at the time were correct.

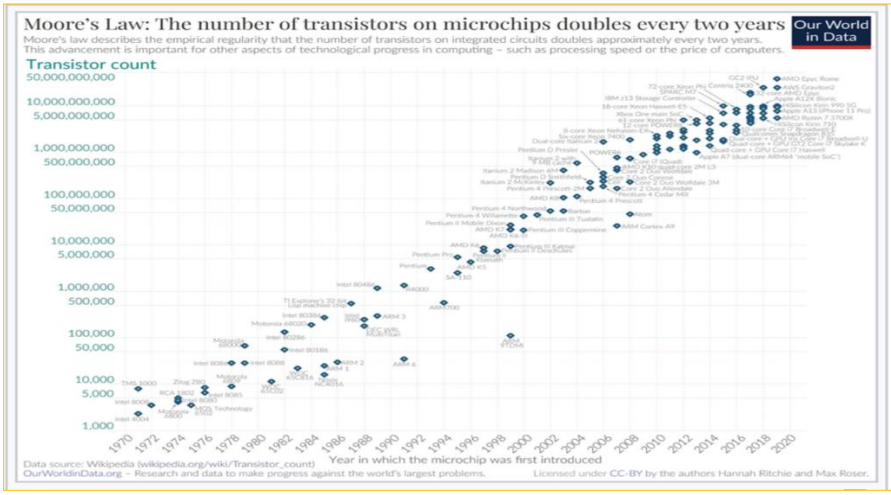

Figure 1. Moore's law projection (Source: OurWorldData.org).

However, since the beginning of 2020, Moore's Law has shown a clear slowdown, with bottlenecks emerging in design, processing, and manufacturing. Therefore, this study hopes to construct a new type of multi-layer glass chip in an innovative way with new ideas.

Discussion

To understand the operation of chip design, one must first start from its structural foundation and understand the operating principles and mechanisms within it. Among them, the most important concept is the principle of least action. The principle of shortest action states that starting from different paths, the shortest distance is ultimately chosen. In the quantum world, this is called "phase," and the phases that appear in different domains are merely fulcrums in the path process, and the laws of physics will ultimately choose the shortest distance. When applied to computer chips, the entire operation maze process is completed with the minimum electronic path. In fact, each chip is like a small city, filled with dense circuits, like a maze. If we observe each chip carefully, we will find that it is filled with diodes, and each diode contains a wafer circuit, It's like an electron trying to complete a process in an electronic maze as quickly as possible and find the exit at each checkpoint. Each row of chips is like a small city, and in the computer world, they call it a domain, an IC. Each IC may vary in size, but the mechanism is the same: the electron must complete a process in the shortest possible time.

Therefore, computer chip design tends to be miniaturized. The reason for miniaturization is to enable electronics to complete the entire process using the shortest possible path. Therefore, the smaller the chip size, the faster the computing speed. And because the entire circuit flow is shorter, the power consumption is also reduced. This is a mutually reinforcing design: power consumption is directly proportional to chip size. The larger the chip size, the higher the power consumption, and vice versa.

As mentioned earlier, according to Moore's Law, chips will be upgraded every 18 to 24 months, and the size of the chip will be smaller than the previous generation, usually half the size. In other words, according to Moore's Law, the size of the chip will be reduced by half every 18 months. However, this law seems to have been broken in recent years. The speed of chip upgrades has slowed down. Moreover, as chips become smaller, the technical difficulties and technology gaps that arise are also increasing. Even so, it can be said that the chip industry's research and development capabilities have reached a bottleneck. The reasons are as follows:

1) The entire process concept is different, and the same concepts and methods can no longer be used to compress chips. This means that traditional methods have reached their limits.
2) Each chip generation requires a completely new design and manufacturing process. In other words, if the chip design and production methods remain unchanged, it will be impossible to design smaller, faster, and more precise chips. Therefore, this article advocates a new multi-layer manufacturing concept, using a stacked approach to achieve chip multi-layering and multi-layer compression as a solution to chip miniaturization.

The concept of multi-layer chips allows existing chips to be stacked to form more and denser circuits. The characteristic is that multiple electrons can perform independent calculations in their own blocks. Ultimately, multi-layer compressed chips can process more data and more calculations. Multi-layer fully compressed chips may be another viable option for chip miniaturization. Some people may ask whether multi-layer chips will tend to be larger or larger in size. In fact, the answer is no. Even if we start from the concept of building multi-layer chips, we can build chips with smaller size and faster computing speed. This is not limited to research and development and manufacturing but is just a difference in chip manufacturing concepts. Different design schemes and chip designs are derived from chip design concepts. This is the key point brought to you in this article, using multi-layer compression direction instead of the traditional process of only shrinking the area in one direction.

Suggestion

This article's emphasis on multi-layer chip synthesis does not mean abandoning the concept of chip miniaturization. Rather, it represents an effective conceptual approach to addressing the bottlenecks in chip R&D and manufacturing. The concept of multi-layer chips to compress is our innovative idea. This innovative concept is suggested to miniaturization with multi-layer, which was directly fit-into the current chip trend. Therefore, this article proposes a completely new chip design and manufacturing concept, replacing existing chip design and manufacturing methods with the new concept of multi-layer chip compression technology.

One solution is to find a material that conducts faster and more stably than polysilicon. This material must possess both plating and resistivity, yet be faster and more stable than polysilicon. The industry has no alternative but to use superconductors, but superconductors require temperatures above -150 degrees Celsius to function, making this impractical for large-scale household applications. This article proposes the innovative concept of mixing glass fiber with polysilicon, to manufacture chip optical fibers, the "glass core" has the performance of high-speed transmission and multi-dimensional digital transmission, and has high transmission. If glass can be sprayed and mixed with polysilicon, a multi-layer "glass chip" with high transmission and high conductivity can be manufactured. A layer of polysilicon film (such as ITO) is plated on the glass surface, or glass silicon oxide is fused with polysilicon to make them highly compatible, which can become a volume conductive glass core. Spraying can make the "glass core" miniaturized, and multi-layering can be realized.

Furthermore, glass cores exhibit total internal reflection, which increases the speed of light transmission. When combined with polysilicon, they can achieve dual-track operation for both optical and electronic transmission. This "glass core" can overcome current industry bottlenecks, breaking the decades-long tradition of single-path chip design. Multi-layer compression, miniaturization, and the integration of glass fiber and polysilicon are the only viable path to future high-capacity chip manufacturing. Therefore, the innovative proposals presented in this article are worthy of consideration by the computer and electronics industries.

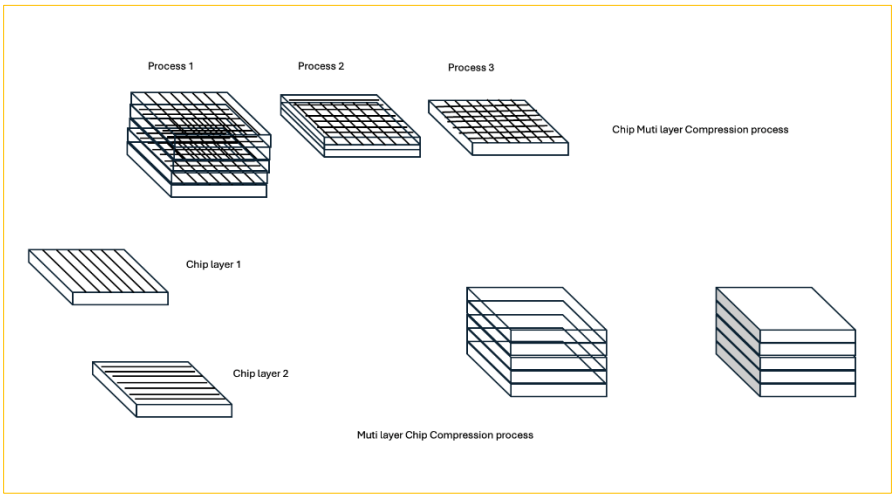

Figure 2. Multi-layer glass + polysilicon chip compression process (Author's view).

More importantly, the "glass core" may be the only way to manufacture quantum computers and popularize them at room temperature. Quantum chips have the characteristic of zero and one simultaneity, that is, zero and one exist at the same time. In computers, the operating elements, that is, one carries light and zero does not carry light, one is charged and zero is uncharged, can coexist in the "glass core". This common property, that is, this simultaneous existence, makes the "glass core" a feasible manufacturing method with compatibility, reliability and stability for the manufacture of quantum chips and quantum computers, which is worthy of industry research.

That mean, the "glass core" may be crucial for developing quantum computers that work at room temperature. Quantum chips can hold zero and one states simultaneously, meaning both coexist at the same time. In classical computers, the basic elements-where light indicates one and the absence of light indicates zero, with one charged and zero uncharged-can be integrated within the "glass core." This characteristic, the ability to exist in both states simultaneously, makes the "glass core" a promising method for creating quantum chips and computers. It offers advantages such as compatibility, reliability, and stability, making it an attractive focus for computer chip research.

So, in other words, the "glass core" could be the key to manufacturing quantum computers and making them accessible at room temperature. Quantum chips have the property of zero and one existing simultaneously, meaning zero and one coexist at the same time. In computers, the operating elements-where one carries light and zero does not, with one being charged and zero uncharged-can coexist within the "glass core." This shared feature, the simultaneous existence of both states, makes the "glass core" a viable method for producing quantum chips.

Conclusion

This article explores Moore's Law limitations in the modern semiconductor industry. A deceleration trend shows increased latency in development cycles for new generations, indicating a deviation from projections and a potential breach of Moore's Law. This highlights the need for paradigm shifts in research, design, manufacturing, and the exploration of new materials and architectures. To effectively overcome these challenges, this paper advocates an innovative and comprehensive approach centered on the development and implementation of hierarchical, multi-layered chip architectures. These architectures leverage state-of-the-art materials, such as glass-core multi-layer structures fabricated from emerging and advanced semiconductor compounds, to enhance performance, scalability, and reliability in next-generation electronic systems. This approach aims to enhance integration density, thermal management, and electrical performance, thereby pioneering a new trajectory for semiconductor evolution. The implementation of such multi-layered, composite chips could potentially redefine industry standards and catalyze the development of next-generation computing systems, providing a robust pathway to sustain Moore's Law's underlying principles in a post-legacy era.

Declarations

Acknowledgments: The author would like to acknowledge the independent nature of this research, which was conducted without institutional or external support.

Author Contribution: The author confirms sole responsibility for the following: study conception and design, data collection, analysis and interpretation of results, and manuscript preparation.

Conflict of Interest: The author declares no conflict of interest.

Consent to Publish: The author agrees to publish the paper in International Journal of Recent Innovations in Academic Research.

Data Availability Statement: All relevant data are included in the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Research Content: The research content of the manuscript is original and has not been published elsewhere.

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1. OurWorldData.org

Citation: Lie Chun Pong. 2025. Innovative “Multi-Layered Glass Chip” (Glass Plus Polysilicon Chip) as the New Standard for the Future of the Computer Industry. International Journal of Recent Innovations in Academic Research, 9(3): 149-152.